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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/183,389	10/29/1998	VLADIMIR BEREZIN	08305/048001	3070

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EXAMINER
WHIPKEY, JASON T

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 07/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/183,389	Applicant(s) BEREZIN, VLADIMIR	
	Examiner Jason T. Whipkey	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

✓2. Claim 6 is objected to because of the following informality: The phrase "integrated digitally integrated digital image data" on lines 23-24 is unclear. Appropriate correction is required.

✓3. Claim 8 is objected to because of the following informality: "Using" is misspelled as "uaing" on line 3. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Merrill (U.S. Patent No. 5,892,541).

Merrill teaches that an active pixel cell 200 may be formed on a substrate 210, shown in Figure 7 (column 11, lines 45-46). Cell 200 is a schematic view of cell 110 shown in Figure 3 (column 11, lines 40-42). As shown in Figure 2, each cell 110 — which is part of imaging system 100 — is connected to an output line CO (column 4, lines 62-66).

Each cell 110 is sampled *n* times during each integration cycle (column 6, lines 56-59). Each integration period may be 30 ms, which is approximately equal to the NTSC standard frame display time of 1/30 of a second. Detection circuits DC1-DCm digitize the partial integration voltages from each cell 110 (column 7, lines 27-31). Memory unit 112 stores the partial digital integration values and totals them, forming a total digital integration value (column 8, lines 51-54). In order for this process to be useful, it is inherent that this aggregate image is then output.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Fossum.

Regarding claim 1, Merrill teaches that an active pixel cell 200 may be formed on a substrate 210, shown in Figure 7 (column 11, lines 45-46). Cell 200 is a schematic view of cell 110 shown in Figure 3 (column 11, lines 40-42). As shown in Figure 2, each cell 110 — which is part of imaging system 100 — is connected to an output line CO (column 4, lines 62-66). Each cell 110 is sampled *n* times during each integration cycle (column 6, lines 56-59). This sampling determines the number of photons collected in the cell since its last reset (column 3, lines 47-49). Memory unit 112 stores partial digital integration values from the cells and totals them, forming a total digital integration value (column 8, lines 51-54).

Merrill is silent with regard to placing the active pixel cells on the same substrate as the memory.

Fossum discloses a focal plane array 12 with CMOS pixels (column 6, lines 15-18) and a buffer memory 23, shown in Figure 7. The system shown in Figure 7 may be monolithic (column 9, lines 52-54). As stated in column 9, lines 63-65, the advantage to using a monolithic architecture is that performance is increased. For this reason, it would be obvious to have Merrill's system formed on a single substrate.

Regarding claim 2, Merrill teaches that detection circuits DC1-DCm digitize the partial integration voltages from cells 110 before outputting them to memory unit 112 (column 7, lines 27-31).

Regarding claim 4, each cell 110 is sampled multiple times during each integration cycle (column 10, lines 6-8). As shown in Figure 5, this sampling allows the total collected photon value to exceed the maximum capacity of the cell (column 10, lines 11-16).

Regarding claim 5, Merrill is silent with regard to fixed pattern noise reduction being performed before A/D conversion.

Fossum discloses that each pixel has self-biasing circuitry to reduce reset noise (column 8, lines 44-47). Noise is therefore reduced after the image is sensed but before digital counters 21 digitize the signal. The advantage to reducing a signal's noise before digitizing the signal is that the digital signal produced is a more accurate representation of the intended image. For this reason, it would have been obvious to have Merrill's system implement noise reduction circuitry before digitizing the signals.

Regarding claim 6, Merrill teaches that an active pixel cell 200 may be formed on a substrate 210, shown in Figure 7 (column 11, lines 45-46). Cell 200 is a schematic view of cell 110 in Figure 3 (column 11, lines 40-42). As shown in Figure 2, each cell 110 — which is part of imaging system 100 — is connected to an output line CO (column 4, lines 62-66). Each cell 110 is sampled multiple times during each integration cycle (column 10, lines 6-8). This sampling determines the number of photons collected in the cell since its last reset (column 3, lines 47-49). As shown in Figure 5, the sampling also allows the total collected photon value to exceed the maximum capacity of the cell (column 10, lines 11-16).

Detection circuits DC1-DCm digitize the partial integration voltages from cells 110 before outputting them to memory unit 112 (column 7, lines 27-31). Each integration period is divided into a number of collection periods (column 7, lines 5-12). After all collection periods (and therefore the entire integration period) has concluded, memory unit 112 stores partial digital integration values from the cells and totals them, forming a total digital integration value (column 8, lines 51-54).

Merrill is silent with regard to using a noise reduction circuit between the image sensor and the A/D converter and placing the image sensor, noise reduction circuit, A/D converter, and memory on the same substrate.

Fossum discloses a system comprised of CMOS pixels in focal plane array 12 (column 6, lines 15-18), digital counters 21 that perform A/D conversion (column 9, lines 26-27), and a memory 23, as shown in Figure 7. Each pixel has self-biasing circuitry to reduce reset noise (column 8, lines 44-47). Noise is therefore reduced after the image is sensed but before digital counters 21 digitize the signal. The advantage to reducing a signal's noise before digitizing the signal is that the digital signal produced is a more accurate representation of the intended image. For this reason, it would have been obvious to have Merrill's system implement noise reduction circuitry before digitizing the signals.

Fossum also discloses that all of the above-mentioned circuits, shown in Figure 7, may be monolithic (column 9, lines 52-54). As stated in column 9, lines 63-65, the advantage to using a monolithic architecture is that performance is increased. For this reason, it would be obvious to have Merrill's system formed on a single substrate.

Regarding claim 7, cells 110 are active pixel sensor cells (column 4, line 50).

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (U.S. Patent No. 5,892,541) in view of Fossum and further in view of Mandl.

Claim 3 may be treated like claim 2, as described above. However, both Merrill and Fossum are silent with regard to using an oversampling A/D converter.

Mandl shows in Figures 3A and 3B a video camera that uses an oversampling A/D converter (column 4, line 67 through column 5, line 3). A/D converter 144 in Figure 3B digitizes charges from array column 156 (column 5, line 67 through column 6, line 16). The charges from array column 156 are oversampled (column 6, lines 50-56). As stated in column 10, lines 14-20, an oversampling A/D converter in an imaging system improves image quality. For this reason, it would have been obvious to have Merrill's system utilize an oversampling A/D converter.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703)

305-1819. The examiner can normally be reached Monday through Friday from 8 A.M. to 5:30 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned are (703) 872-9314 for both regular communication and After Final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to (703) 872-9314 for either formal or informal communications intended for entry. (For informal or draft communications, please label "**PROPOSED**" or "**DRAFT**".)

Hand-delivered responses should be brought to the sixth floor receptionist of Crystal Park II, 2121 Crystal Drive in Arlington, Virginia.

JTW

JTW
July 15, 2002

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600